## REMARKS

Claims 1-20, all the claims pending in the application, stand rejected on prior art grounds. Claims 1-3, 8-9, 11-12, and 14-15 are amended herein. Moreover, the specification is objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

### I. The Objection to the Specification

The abstract of the disclosure is objected to because of informalities. Accordingly, the Applicants have amended the abstract to remove the title of the invention in accordance with the suggestion in the Office Action. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objection to the specification.

### II. The Prior Art Rejections

Claims 1-4, 8-10, and 14-16 stand rejected under 35 U.S.C. §102(c) as being anticipated by Kirsch (U.S. Patent No. 6,812,799). Claims 5-7, and 17-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kirsch, in view of Goto (U.S. Patent No. 3,555,194). Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kirsch, in view of Stubbs, et al. (U.S. Publication No. 2002/0057119), hereinafter referred to as Stubbs. Claims 12 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kirsch, in view of Stubbs, in further view of Goto. Applicants respectfully traverse these rejections based on the following discussion.

Kirsch teaches a synchronous mirror delay including a ring oscillator that generates a plurality of tap clock signals with one tap clock signal being designated an oscillator clock



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signal. In response to an input clock signal, a model delay line generates a model delayed clock signal having a model delay relative to the input clock signal. A coarse delay circuit generates a coarse delay count responsive to the oscillator, input, and model delayed clock signals, and activates a coarse delay enable signal responsive to the delay count being equal to a reference count value. A fine delay circuit latches the tap clock signals and develops a fine delay from the latched signals, and activates a fine delay enable signal having the fine delay in response to the coarse delay enable signal. An output circuit generates a delayed clock signal responsive to the coarse and fine delay enable signals going active.

Goto teaches an interstation synchronization apparatus for a time division multiplex communication system having a plurality of communication stations is provided wherein multi-in-put, phase-controlled oscillator means, whose output signal represents the station synchronization signal, is present at each station therein. The multi-input, phase-controlled oscillator means is synchronized by a comparison of the synchronization signal generated thereby with synchronization signals generated at stations remotely located therefrom. The multi-input phase-controlled oscillator means is compensated for phase lags present in the externally generated synchronization signals as applied thereto by discrete signal levels introduced therein to control the frequency of the output signal thereof.

Stubbs teaches a delay locked loop having improved synchronization times having a variably adjustable delay line which accepts two incoming clock pulses. As each pulse propagates through the delay line an edge of the pulse toggles or retoggles a shift bit corresponding to a delay element. When the first pulse reaches the end of the delay line, the status of the shift bits is frozen, and a starting point for a synchronization sequence begins at the transition point between toggled and retoggled shift bits.



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The claimed invention, as provided in amended independent claims 1, 8, and 14 include features, which are patentably distinguishable from the prior art references of record. Specifically, claim 1 recites, in part, "...a binary-weighted delay circuit operable to receive said first clock signal and to produce a delayed clock signal; a phase-shifted delay circuit connected to said binary-weighted delay circuit; and a latch element connected to said binary-weighted delay circuit, said latch element operable to check whether said delayed clock signal is delayed by an amount equal to said desired cycle time, wherein delay elements of said binary-weighted delay circuit are intermixed with delay elements of said phase-shifted delay circuit."

Furthermore, claim 8 recites, in part, "...a first delay circuit receiving said first clock line and outputting a delayed clock signal, wherein said first delay circuit comprises a binary-weighted delay circuit; a second delay circuit receiving said delayed clock signal and producing a phase shift of said delayed clock signal; and a latch element operatively connected to said first delay circuit, wherein said latch element compares whether said delayed clock signal is delayed by an amount equal to said desired cycle time, wherein delay elements of said first delay circuit are intermixed with delay elements of said second delay circuit, and wherein said second delay circuit is configured as an exact multiple of said first delay circuit."

Moreover, claim 14 recites, in part, "...sending said first clock signal to a binary-weighted delay circuit; generating a delayed clock signal in said binary-weighted delay circuit; comparing a delay of said delayed clock signal with said desired cycle time in a latch element, wherein said binary-weighted delay circuit comprises said latch element; and generating a phase shift of said delayed clock signal in a phase-shifted delay circuit, wherein delay elements of said binary-weighted delay circuit are intermixed with delay elements of said phase-shifted delay circuit, and wherein said phase-shifted delay circuit is configured as an exact multiple of said



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binary-weighted delay circuit."

As indicated above, the Applicants' claimed invention is patentably distinct from Kirsch. Although some circuit blocks are common between the Applicants' claimed invention and Kirsch (up/down counters, compare circuits), the implementation is significantly different between the two. The Applicants' invention provides a binary-weighted delay chain that is programmed to match the external clock period. The matching is achieved by compressing or stretching the delay of every binary-weighted inverter within the chain. In other words, the propagation delay of each inverter in the chain can be adjusted by making the strength of the inverter stronger or weaker. There are no tap points or muxes to accomplish this. Once this delay chain is adjusted to match the delay of the clock period, then separate delay chains having 1/x the number of identical stages (x is the number of stages) is used to provide a phase shift of the main clock. For example, if the main delay chain is programmed to match a cycle time of 4ns, then separate delay chains that are 1/4 in length of the main delay line can be used to provide 1ns delays.

The Office Action contests that the Applicants' clock generation circuitry to produce two rising clock edges equal to the clock period is covered by Fig. 3 of Kirsch (see page 2 of the Office Action). However, the Applicants respectfully disagree and contend that Fig. 3 of Kirsch does not show the Applicants' claimed circuitry replicated in Fig. 3 therein. Moreover, the Office Action indicates that the Applicants' plurality of "binary-weighted" inverters is also used in Kirsch in elements 302 of Fig. 3 (see page 3 of the Office Action). However, a closer inspection of Fig. 3 of Kirsch and the description thereof shows that the delay 302 is a regular inverter chain with tap points on each output. Conversely, the Applicants' claimed delay element does not have this. In fact, the generation of the phase shifted clocks is accomplished



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quite differently between the Applicants' claimed invention and Kirsch. Specifically, in the Applicants' claimed invention, separate delay chains that are a fraction of the length of the main delay chain are used.

In view of the foregoing, the Applicants respectfully submit that the collective cited prior art references do not teach or suggest the features defined by amended independent claims 1, 8, and 14 and as such, claims 1, 8, and 14 are patentable over Kirsch, Goto, and Stubbs individually or collectively. Furthermore, dependent claims 2-7, 9-13, and 15-20 are similarly patentable over Kirsch, Goto, and Stubbs individually or collectively, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

## III. Formal Matters and Conclusion

With respect to the objection to the specification, the specification (abstract) has been amended, above, to overcome this objection. With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the



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Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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